1. Using D flip-flops and logic gates, design a counter that outputs the following sequence: 00, 01, 10, 00, 01, 10…. (We don’t care what happens if the counter is somehow forced into the unwanted state 11.)

A. How many flip-flops do you need? Two.

B. Write out the necessary truth table, showing how Next State depends on Present State.

<table>
<thead>
<tr>
<th>Present State</th>
<th>Next State</th>
</tr>
</thead>
<tbody>
<tr>
<td>q1</td>
<td>q0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

C. (Two points.) Write a logic equation for each bit’s Next State.

D0 = ~(q1 \| q0)

D1 = ~q1 \& q0

D. If the initial state is 11, what will the next state be (according to your logic equations)? 00

E. (Two points.) Write out the circuit diagram.

![Circuit Diagram](image-url)
2. Using D flip-flops and logic gates, design a Mealy machine that detects the sequence 0101.

A. First, list all the states (s0, s1, etc.) that we need to define, and briefly define them.

s0: nothing detected
s1: first 0 detected
s2: 01 detected
s3: 010 detected

B. (Four points.) Write out the state diagram (not the circuit diagram).

C. How many flip-flops do you need? 2

D. Write out the necessary truth table, showing how Next State and Output depend on Present State and Input.

<table>
<thead>
<tr>
<th>q1</th>
<th>q0</th>
<th>In</th>
<th>D1</th>
<th>D0</th>
<th>Out</th>
</tr>
</thead>
<tbody>
<tr>
<td>s0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>s0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>s1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>s1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>s2</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>s2</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>s3</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>s3</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>
E. (Three points.) Write a logic equation for each bit's Next State and for the Output.

\[ D_0 = \neg \text{In} \]
\[ D_1 = q_0 \& \text{In} \mid q_1 \& \neg q_0 \& \neg \text{In} \]
\[ \text{Out} = q_1 \& q_0 \& \text{In} \]

F. (Three points.) Write out the circuit diagram.