Name:_____

Honor Pledge: I am adhering to the Honor Code while taking this test.

Signature:_____ Date:_____

1. Using D flip-flops and logic gates, design a counter that outputs the following sequence: 00, 01, 10, 00, 01, 10…. (We don't care what happens if the counter is somehow forced into the unwanted state 11.)

A. How many flip-flops do you need? Two.

B. Write out the necessary truth table, showing how Next State depends on Present State.

Present State		Next State	
q1	q0	D1	D0
0	0	0	1
0	1	1	0
1	0	0	0

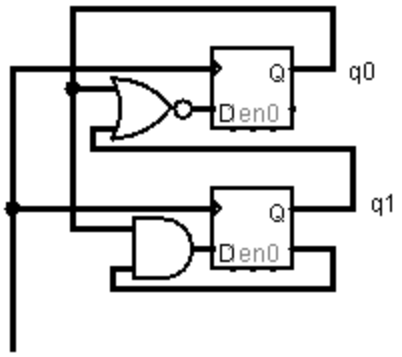
C . (Two points.) Write a logic equation for each bit's Next State.

D0 = ~(q1 | q0)

D1 = ~q1 & q0

D. If the initial state is 11, what will the next state be (according to your logic equations)? 00

E. (Two points.) Write out the circuit diagram.



2. Using D flip-flops and logic gates, design a Mealy machine that detects the sequence 0101.

A. First, list all the states (s0, s1, etc.) that we need to define, and briefly define them.

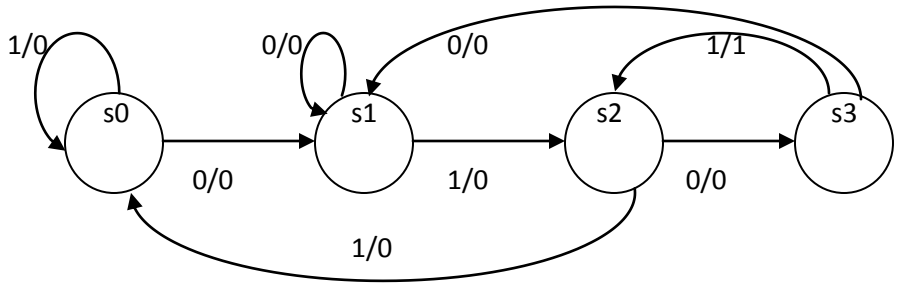
s0: nothing detected

s1: first 0 detected

s2: 01 detected

s3: 010 detected

B. (Four points.) Write out the state diagram (not the circuit diagram).



C. How many flip-flops do you need? 2

D. Write out the necessary truth table, showing how Next State and Output depend on Present State and Input.

	q1	q0	In	D1	D0	Out
s0	0	0	0	0	1	0
s0	0	0	1	0	0	0
s1	0	1	0	0	1	0
s1	0	1	1	1	0	0
s2	1	0	0	1	1	0
s2	1	0	1	0	0	0
s3	1	1	0	0	1	0
s3	1	1	1	1	0	1

E. (Three points.) Write a logic equation for each bit's Next State and for the Output.

D0 = ~In

D1 = q0&In | q1&~q0&~In

Out = q1 & q0 & In

F. (Three points.) Write out the circuit diagram.