Name:_____

Honor Pledge: I am adhering to the Honor Code while taking this test.

Signature:_____ Date:_____

25 points total.

1. (One point.) **10101010** is the two's complement representation of what base 10 number?

-128+32+8+2 = -86

2. (Six points.) Compute the sums, indicating the values of the carry and overflow flags.

```
  10101010
 +10101010
  01010100        Carry: 1    Overflow: 1
```

```
  01010101
 +01010101
  10101010        Carry: 0    Overflow: 1
```

3. (Five points.) The trustees of Karnaugh University (Alice, Bob, Carol, and David) are at it again! They're voting on a proposal to eliminate the physics department, in retaliation for certain instances of irreverent humor. If the number of YES votes (to eliminate the physics department) is 2 or 3, the physics department will be eliminated. If the number of YES votes is 0, the physics department will be saved. If the number of YES votes is 1, the University doesn't care whether the physics department is eliminated or saved. (However, to save money, the University prefers to use only one logic gate in the circuit that indicates the outcome of the vote.)

A. Complete this truth table, where 1 as an input represents a YES vote, and 1 as an output represents the elimination of the physics department. X as an output represents "don't care."

A	B	C	D	ELIMINATE
0	0	0	0	0
0	0	0	1	X
0	0	1	0	X
0	0	1	1	1
0	1	0	0	X
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	X
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

B. Write out a K map equivalent to the truth table.

		CD			
		00	01	11	10
AB	00	**0**	**X**	**1**	**X**
	01	**X**	**1**	**1**	**1**
	11	**1**	**1**	**1**	**1**
	10	**X**	**1**	**1**	**1**

C. Write out any logic equation that implements the truth table. (You may use as many gates as you like.)

ELIMINATE = A + B + C + D

D. Draw the circuit diagram equivalent to your response to part C.

A four-input OR.

E. Write out a logic equation that implements the truth table using only one gate. (What's good for logic minimization may be bad for the physics department.) Your responses to C and E may be identical.

ELIMINATE = A + B + C + D

4. Harry, Hermione, and Ron are voting to decide whether to skip their final year at Hogwarts. A 1 is a vote to skip Hogwarts (and instead to hunt Horcruxes and battle Death Eaters). **Harry's vote counts twice**: consider the sum of Harry's vote and Harry's vote (again) and Hermione's vote and Ron's vote. The output of a circuit is 1 if the sum is 2, 3, or 4; the output is 0 if the sum is 0 or 1. The inputs are Harry's, Ron's, and Hermione's votes. Your task is to construct the circuit using logic gates—the future of Hogwarts is in your hands!

A. (One point.) Write out the K map for the necessary circuit.

		HermioneRon			
		00	01	11	10
Harry	0	**0**	**0**	**1**	**0**
	1	**1**	**1**	**1**	**1**

B. (One point.) Write out a minimized logic equation (using as few gates as possible) equivalent to the K map. (Hint: Only two gates are required.)

Output = Harry + (Hermione)(Ron)

C. (One point.) Draw the circuit diagram equivalent to your minimized logic equation.

AND Hermione with Ron, then OR the output with Harry.

D. (Three points.) Write a Verilog module (including the **module** and **endmodule** statements) that uses an **assign** statement to implement your circuit.

```
module partD (input Harry, input Hermione, input Ron, output Q);

assign Q = Harry | (Hermione & Ron);

endmodule
```

E. (Seven points.) Write a Verilog module that computes a sum and uses an **if** statement to implement your circuit.

```
module partE (input Harry, input Hermione, input Ron, output reg Q);

wire [2:0] sum;

assign sum = 2*Harry + Hermione + Ron;

always @ (*)

if (sum < 2) Q = 0;

else Q = 1;

endmodule
```