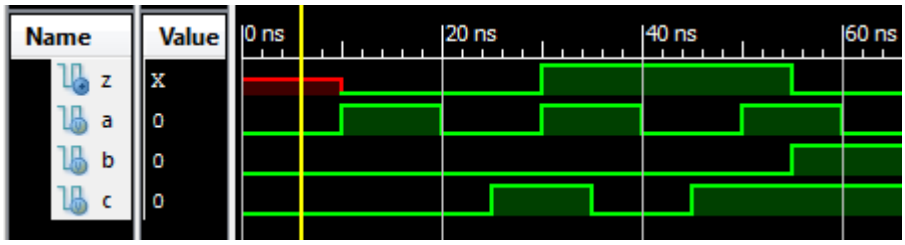
Name:_____

Honor Pledge: I am adhering to the Honor Code while taking this test.

Signature:_____ Date:_____

1. The figure shows the simulation of a D flip-flop. **z** is the output.



A. Which input is normally called "clear" or "reset"?

B. Why is the value of the output unknown before 10 ns?

C. If **b** falls to 0 at 68 ns, while **a** remains at 0 and **c** remains at 1, will the output change?

D. (Five points.) Write a Verilog module (not the test fixture) to implement this circuit.

E. (Two points.) Write a Verilog module to implement a D flip-flop whose output becomes 0 immediately when the clear input goes low (not high); otherwise, the circuit is identical to the previous case.

2. Using D flip-flops and logic gates, design a Mealy machine that detects the sequence 1001.

A. First, list all the states (s0, s1, etc.) that we need to define, and briefly define them.

B. (Four points.) Write out the state diagram (not the circuit diagram).

C. How many flip-flops do you need?

D. Write out the necessary truth table, showing how Next State and Output depend on Present State and Input.

E. (Three points.) Write a logic equation for each bit's Next State and for the Output.

F. (Three points.) Write out the circuit diagram.

G. Write an expression for D0 (as a function of q0, q1, and In) that requires only three logic gates (including NOTs). Your response for part G may be the same as part of your response for part E.

H. Write an expression for D1 (as a function of q0, q1, and In) that requires only three logic gates (including NOTs). Your response for part H may be the same as part of your response for part E.