Using D flip-flops and logic gates, design a Mealy machine that detects the sequence 0010.

A. First, list all the states (s0, s1, etc.) that we need to define, and briefly define them.

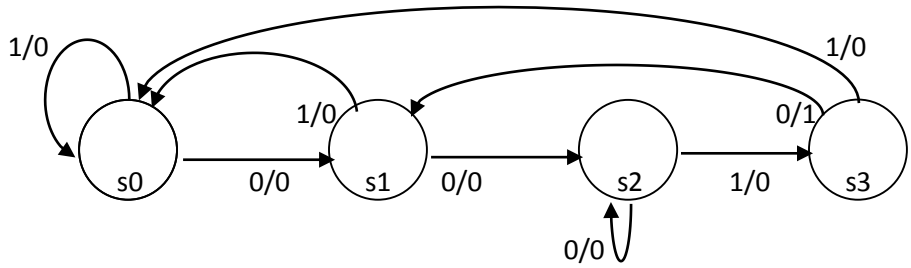
s0: first 0 not detected

s1: 0 detected

s2: 00 detected

s3: 001 detected

B. (Four points.) Write out the state diagram (not the circuit diagram).



C. Write out the necessary truth table, showing how Next State and Output depend on Present State and Input.

	q1	q0	In	D1	D0	Out
s0	0	0	0	0	1	0
s0	0	0	1	0	0	0
s1	0	1	0	1	0	0
s1	0	1	1	0	0	0
s2	1	0	0	1	0	0
s2	1	0	1	1	1	0
s3	1	1	0	0	1	1
s3	1	1	1	0	0	0

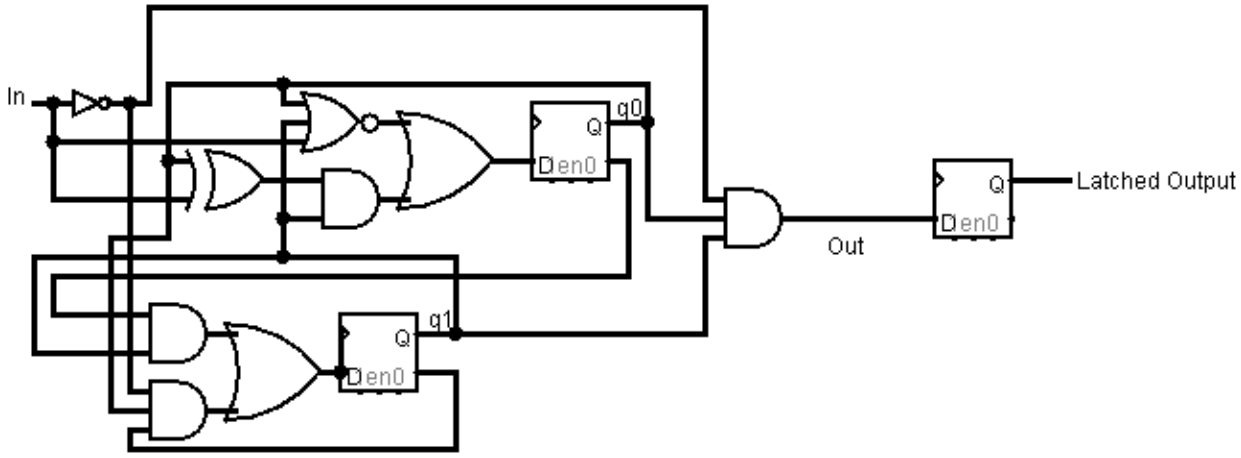
D. (Three points.) Write a logic equation for each bit's Next State and for the Output.

D0 = ~(q0|q1|In) | q1&(q0^In)

D1 = q1&~q0 | ~In&q0&~q1

Out = q1 & q0 & ~In

E. (Three points.) Write out the circuit diagram.



F. (Ten points.) Verilog module

```
module test2 (input clk, input In, output reg LatchedOutput);

reg q0;

reg q1;

always@(posedge clk)

begin

q0 <= ~(q0|q1|In) | q1&(q0^In);

q1 <= q1&~q0 | ~In&q0&~q1;
```

```
LatchedOutput <= q1 & q0 & ~In;

end

endmodule
```