Name:_____

Honor Pledge: I am adhering to the Honor Code while taking this test.

Signature:_____ Date:_____

Using D flip-flops and logic gates, design a Mealy machine that detects the sequence 0100.

A. First, list all the states (s0, s1, etc.) that we need to define, and briefly define them.

B. (Four points.) Write out the state diagram (not the circuit diagram).

C. (Four points.) Write out the necessary truth table, showing how Next State and Output depend on Present State and Input. (Use the necessary number of bits to identify Present State and Next State.)

D. (Three points.) Write any correct logic equation for the Next State of each bit and for the Output.

E. (Three points.) Write out the circuit diagram. You may add a flip-flop at the output.

(Verilog module on back.)

F. (Ten points.) Write a Verilog module to implement your circuit.