Name:_____

Honor Pledge: I am adhering to the Honor Code while taking this test.

Signature:_____ Date:_____

Using D flip-flops and logic gates, design a Mealy machine that detects the sequence 0111.

A. First, list all the states (s0, s1, etc.) that we need to define, and briefly define them.

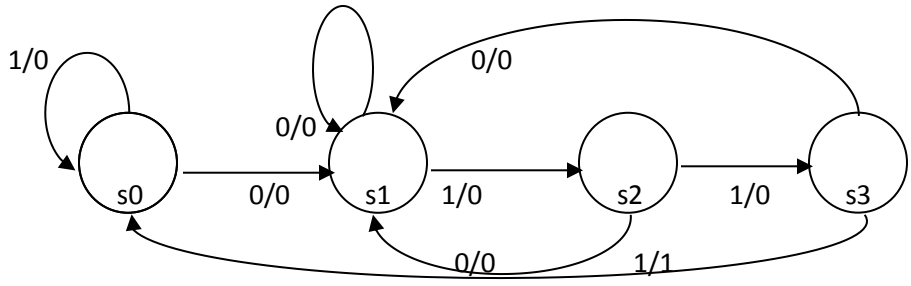
s0: the first 0 has not been detected

s1: 0 detected

s2: 01 detected

s3: 011 detected

B. (Four points.) Write out the state diagram (not the circuit diagram).



C. (Four points.) Write out the necessary truth table, showing how Next State and Output depend on Present State and Input. (Use the necessary number of bits to identify Present State and Next State.)

	q1	q0	In	D1	D0	Out
s0	0	0	0	0	1	0
s0	0	0	1	0	0	0
s1	0	1	0	0	1	0
s1	0	1	1	1	0	0
s2	1	0	0	0	1	0
s2	1	0	1	1	1	0
s3	1	1	0	0	1	0
s3	1	1	1	0	0	1

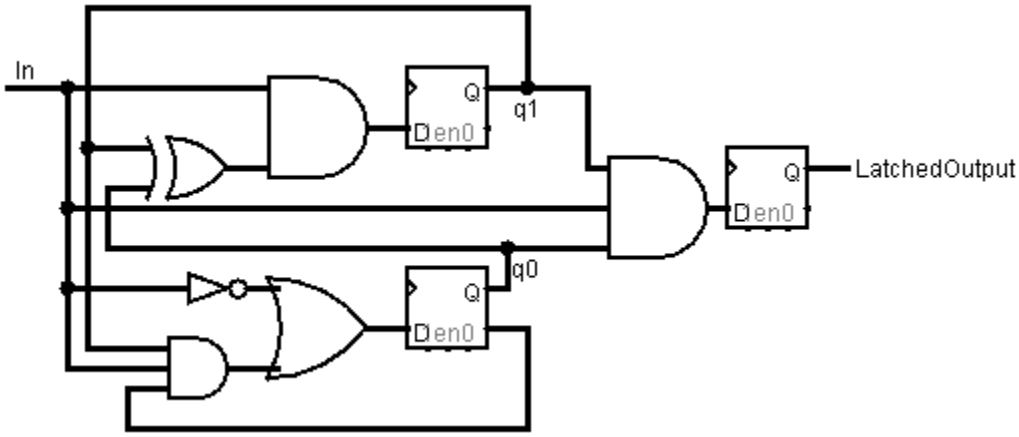
D. (Three points.) Write any correct logic equation for the Next State of each bit and for the Output.

D1 = In&(q1^q0)

D0 = ~In | q1&~q0&In

Out = q1&q0&In

E. (Three points.) Write out the circuit diagram. You may add a flip-flop at the output.



(Verilog module on back.)

F. (Ten points.) Write a Verilog module to implement your circuit.

```
module test2 (input clk, input In, output reg LatchedOutput);

reg q0;

reg q1;

always@(posedge clk)

begin

q0 <= ~In | q1&~q0&In;

q1 <= In&(q1^q0);

LatchedOutput <= q1 & q0 & In;

end

endmodule
```