

Name: _____

Honor Pledge: I am adhering to the Honor Code while taking this test.

Signature: _____

Date: _____

Using D flip-flops and logic gates, design a Moore machine that detects the sequence 101.

A. First, list all the states (s_0, s_1 , etc.) that we need to define, and briefly define them.

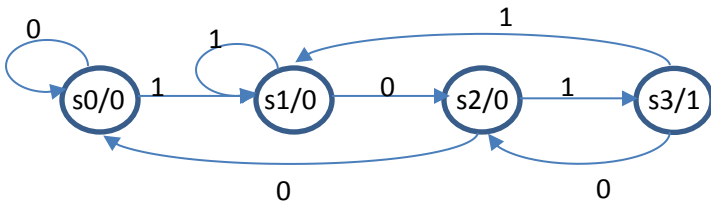
s_0 : nothing useful detected

s_1 : 1 detected

s_2 : 10 detected

s_3 : 101 detected

B. (Four points.) Write out the state diagram (not the circuit diagram).



C. (Four points.) Write out the necessary truth table, showing how Next State and Output depend on Present State and Input. (Use the necessary number of bits to identify Present State and Next State.)

	q1	q0	In	D1	D0	Out
s_0	0	0	0	0	0	0
s_0	0	0	1	0	1	0
s_1	0	1	0	1	0	0
s_1	0	1	1	0	1	0
s_2	1	0	0	0	0	0
s_2	1	0	1	1	1	0
s_3	1	1	0	1	0	1
s_3	1	1	1	0	1	1

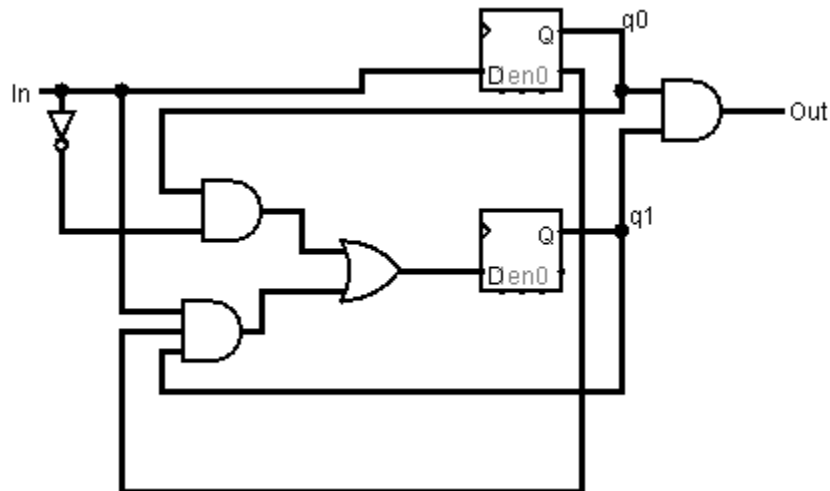
D. (Three points.) Write any correct logic equation for the Next State of each bit and for the Output.

$$\text{Out} = q1 \& q0$$

$$D0 = \text{In}$$

$$D1 = q0 \& \sim \text{In} \mid q1 \& \sim q0 \& \text{In}$$

E. (Three points.) Write out the circuit diagram.



(Verilog module on back.)

F. (Ten points.) Write a Verilog module to implement your circuit.

```
module test2 (input clk, input In, output Out);
```

```
reg q0;
```

```
reg q1;
```

```
assign Out=q0&q1;
```

```
always@(posedge clk)
```

```
begin
```

```
q0 <= In;
```

```
q1 <= q0&~In | q1&~q0&In;
```

```
end
```

```
endmodule
```