Name:_____

Honor Pledge: I am adhering to the Honor Code while taking this test.

Signature:_____ Date:_____

This test is doubled-sided and continues on the back of the second page.

```
module test2 (input clk,
        input In,
        output Out,
        output reg LatchedOutput);
wire D0;
wire D1;
reg q0;
reg q1;
assign D0 = (~q0 |q1 )&~In;
assign D1 = ~In&(q1|q0);
assign Out = q1 & q0 & In;
always@(posedge clk)
begin
q0 <= D0;
q1 <= D1;
LatchedOutput <= Out;
end
endmodule
```

A. (Four points.) Write out the equivalent circuit diagram.

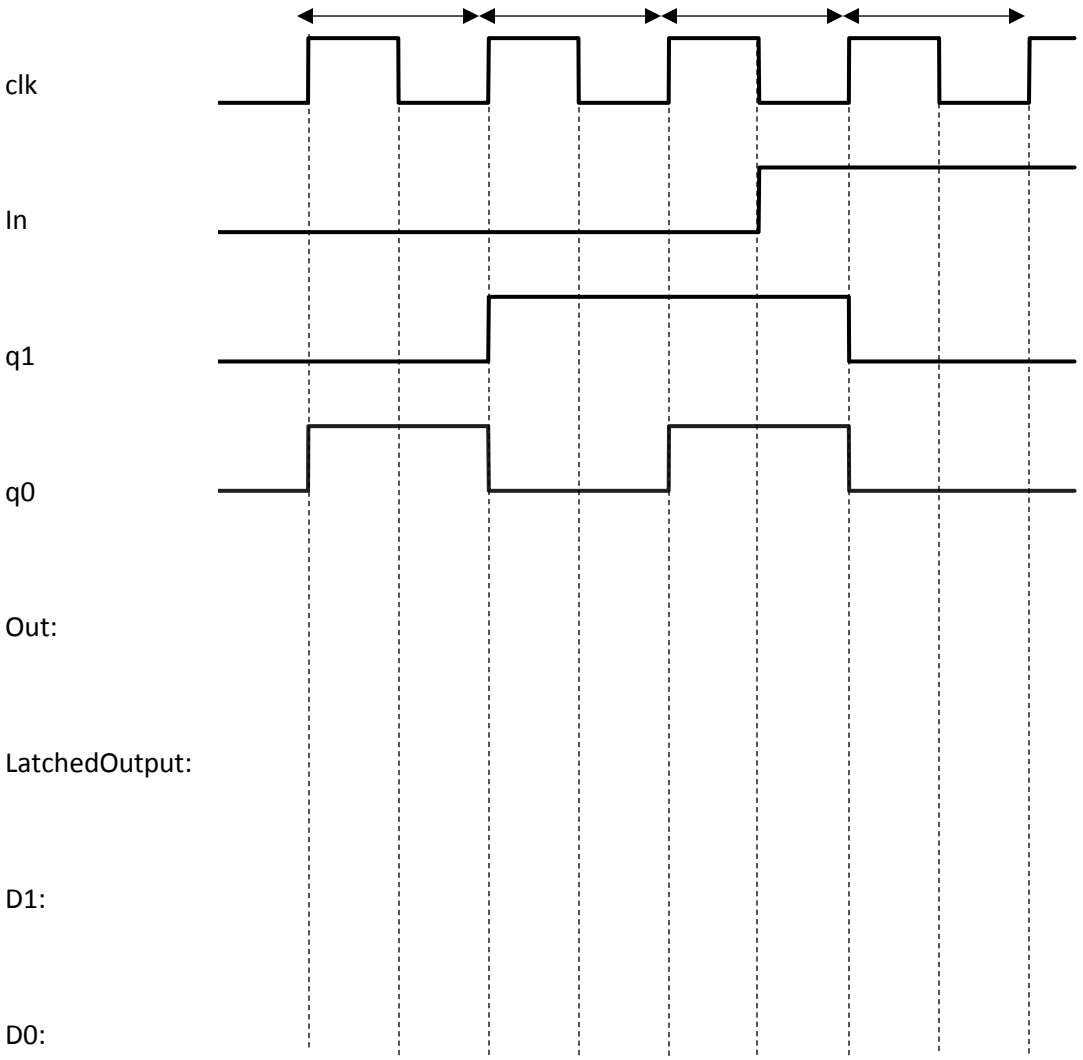
B. (Four points.) Write out the equivalent truth table, showing how Next State (D1, D0) and Out depend on Present State (q1, q0) and In.

C. (Four points.) Write out the state diagram for the Mealy machine that implements the truth table. Label the states s0, s1, s2, and s3.

D. (Four points.) Recognizing that the circuit is a sequence detector, briefly define the states s0, s1, s2, and s3. In other words, in each state, what sequence has just been detected?

E. What sequence does this circuit detect?

F. (Four points.) Over each double-headed arrow, label the state (s0, s1, s2, or s3). Some states may appear more than once or not at all.



G. (Four points.) Add Out, LatchedOutput, D1, and D0 to the timing diagram above, at least over the interval spanned by the four double-headed arrows.