Name:_____

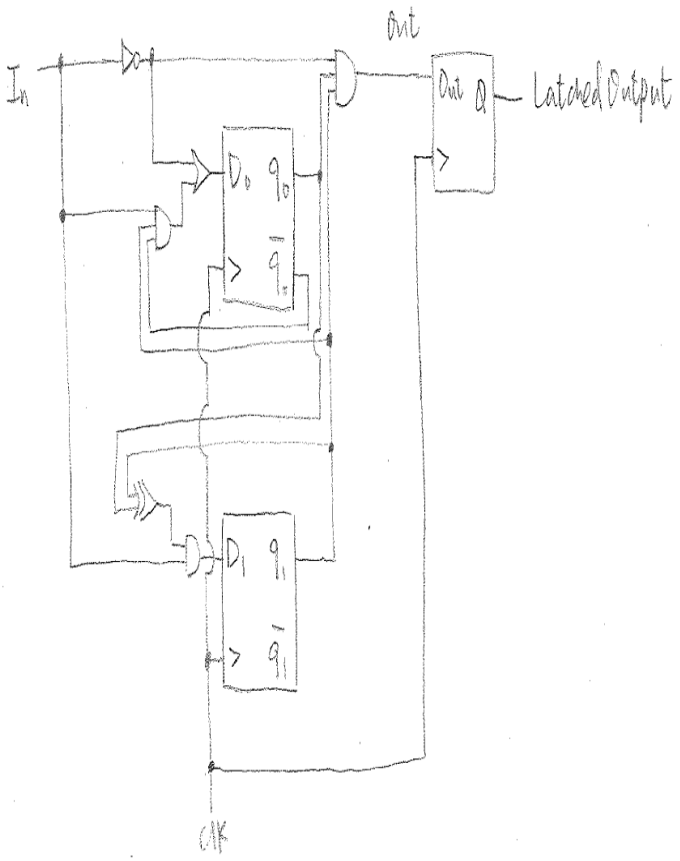
Honor Pledge:  I am adhering to the Honor Code while taking this test.

Signature:_____ Date:_____

```
module test2 (input clk, input In, output Out, output reg LatchedOutput);
wire D0;
wire D1;
reg q0;
reg q1;
assign D0 = ~In | q1&~q0&In;
assign D1 = In&(q1^q0);
assign Out = q1 & q0 & ~In;
always@(posedge clk)
begin
q0 <= D0;
q1 <= D1;
LatchedOutput <= Out;
end
endmodule
```

A. (Four points.) Write out the circuit diagram equivalent to the module.

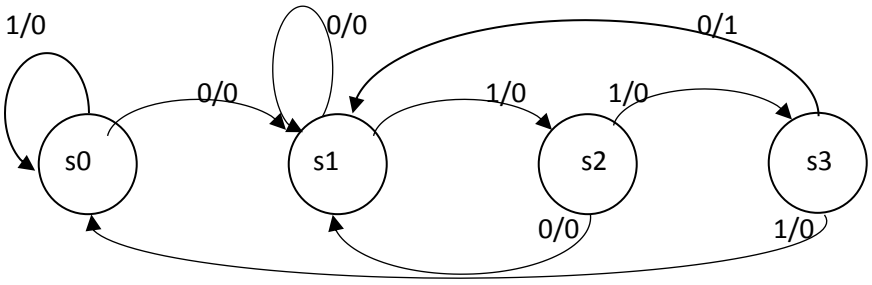
Student solution: very neat, though the OR and XOR gates look funny.



B. (Four points.) Write out the equivalent truth table, showing how Next State (D1, D0) and Output depend on Present State (q1, q0) and Input.

| | q1 | q0 | In | D1 | D0 | Out |
|---|---|---|---|---|---|---|
| s0 | 0 | 0 | 0 | 0 | 1 | 0 |
| s0 | 0 | 0 | 1 | 0 | 0 | 0 |
| s1 | 0 | 1 | 0 | 0 | 1 | 0 |
| s1 | 0 | 1 | 1 | 1 | 0 | 0 |
| s2 | 1 | 0 | 0 | 0 | 1 | 0 |
| s2 | 1 | 0 | 1 | 1 | 1 | 0 |
| s3 | 1 | 1 | 0 | 0 | 1 | 1 |
| s3 | 1 | 1 | 1 | 0 | 0 | 0 |

C. (Four points.) Write out the equivalent state diagram. Label the states s0, s1, s2, and s3.




D. (Four points.) Recognizing that the circuit is a sequence detector, briefly define the states s0, s1, s2, and s3. In other words, in each state, what sequence has just been detected?

s0: no part of sequence detected

s1: 0 detected

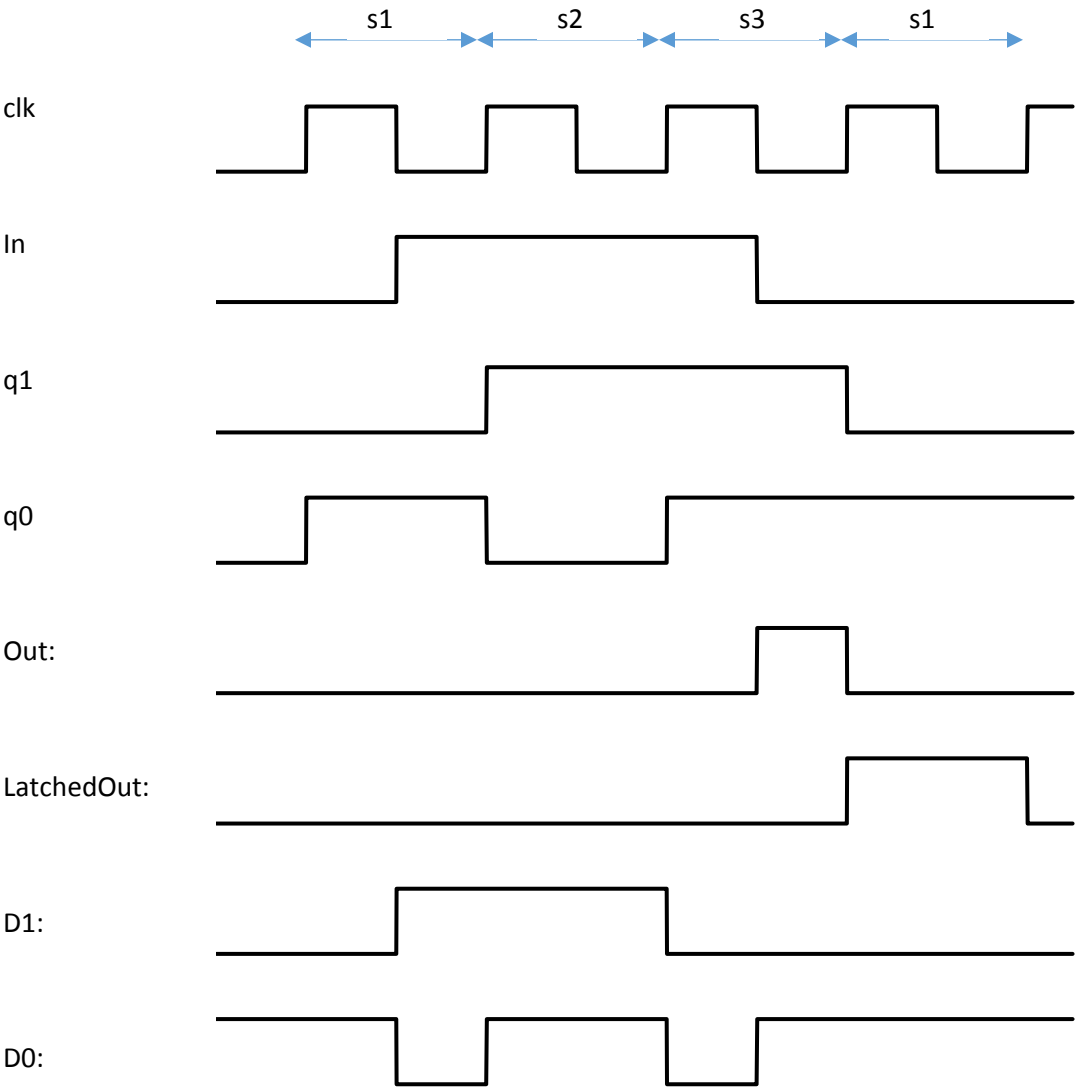
s2: 01 detected

s3: 011 detected

E. What sequence does this circuit detect?

0110

F. (Four points.) Over each double-headed arrow, label the state (s0, s1, s2, or s3).




G. (Four points.) Add Out, LatchedOutput, D1, and D0 to the timing diagram, at least over the interval spanned by the four double-headed arrows.